Storage Class Memory: Opportunities and Challenges

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“Beyond CMOS: From Devices to Systems”
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Disclaimer:
This talk provides an overview of various techniques and concepts, some or all of which may not necessarily reflect what WDC will actually choose using in their products and technologies.
Outline

1. Introducing the New Western Digital

2. System Challenges for Emerging NVMs
   - Industry/Technology Trends
   - Available technologies | The latency vs. cost view
   - Different workloads leading to higher memory complexity

3. Limitations of Current Programming Models

4. Opportunities: Memory Centric Computing
   - A change of perspectives

5. Conclusions | Challenges
   - ..And a few words about commercialization...
The Western Digital Family of Brands

Delivering the Possibilities of Data to Life
A Global Leader in Storage Technology

**LTM Revenue**

Source: Company website; Public filings; analyst reports; S&P Capital IQ

1 Last 4 quarters ending Sep 30, 2016 for WDC, Seagate, Toshiba, Samsung, Micron and SK Hynix; ending Oct 1, 2016 for Intel; ending Oct 28, 2016 for NetApp; and ending Jun 30, 2016 for EMC

2 For the LTM, Toshiba revenue converted to USD at an average exchange rate of 111.78 JPY/USD; Samsung and SK Hynix revenue converted to USD at an average exchange rate of 1160.00 KRW/USD

3 Includes Non-Volatile Memory (Trade and Non-Trade) and Other
Moving Mountains of Data

<table>
<thead>
<tr>
<th></th>
<th>Core Register</th>
<th>Core L1 Cache</th>
<th>Core L2 Cache</th>
<th>Shared L3 Cache</th>
<th>DRAM</th>
<th>Storage Class Memory</th>
<th>Flash</th>
<th>HDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>64KB</td>
<td>256KB</td>
<td>2-4MB</td>
<td>16-128GB</td>
<td></td>
<td>128GB-1TB</td>
<td>512GB-4TB</td>
<td>4-16TB</td>
</tr>
<tr>
<td>Speed</td>
<td>1ns</td>
<td>3-10ns</td>
<td>10-20ns</td>
<td>50-100ns</td>
<td></td>
<td>250-5,000ns</td>
<td>100,000ns-2,000,000ns</td>
<td>5-10,000,000ns</td>
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<tr>
<td>Cost</td>
<td></td>
<td></td>
<td></td>
<td>100x</td>
<td></td>
<td>20-25x</td>
<td>5x</td>
<td>1x</td>
</tr>
</tbody>
</table>
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   - The New Western Digital

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2020 Memory Taxonomy (Conventional)

- **Cost**
  - Cold Storage: NAND, HDD, Tape
  - Storage: NAND, HDD
  - SCM/Persistent Memory (New): ReRAM, PCM
  - Main Memory: DRAM, STT-MRAM
  - Cache: DRAM STT-MRAM
  - Logic: SRAM, eDRAM, STT-MRAM

- **Performance**
  - Reg
  - Embed
  - Cache
  - Main Memory
  - SCM/Persistent Memory (New)

- **2020 Memory Taxonomy**
  - Conventional
DRAM & NAND Cell Sizes

Source: Western Digital estimates

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From the Suburbs to Downtown

2D NAND Architecture

3D NAND Architecture
The BiCS Scaling March

BiCS1

24L

BiCS2

48L

BiCS3

64L

BiCS4

BiCS5

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Cost Scaling for SCM Market Adoption

Cost ($) [LogScale] vs. Year

2016 to 2025:
- DRAM: ~2x change
- SCM: ~20x change
- BiCS: Stabilizing trend

Note: Technology transition cadence assumed 18 months for all technologies.
- ReRAM & 3DXP greenfield fabs, NAND & DRAM existing fabs
- * DRAM data source: IDC ASP forecast with 45% GM assumed
- ** 13 nm: assumes EUV @ 1.4x i-ArF capex cost, 2160 w/day

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Emerging NV Memory Cell Options

**RRAM** Ionic Motion

**Filamentary**
- CBRAM: Cation (Cu, Ag Ion) filament
- OxRAM: Anion (Oxygen Ion) filament

**Non-Filamentary**
- PCMO: Anion (Oxygen Ion) migration
- CERAM: Bulk electronic state (mott transition)
- CNT: Carbon nanotubes

**FLASH**
- Electrons stored in floating gate or charge trap

**MRAM**
- Magnetic tunnel junction

**PCM**
- Phase change

**CBRAM**
- Cation (Cu, Ag Ion) filament

**OxRAM**
- Anion (Oxygen Ion) filament

**PCMO**
- Anion (Oxygen Ion) migration

**CERAM**
- Bulk electronic state (mott transition)

**CNT**
- Carbon nanotubes

3-Terminal Device Variable Threshold Switch

2-Terminal Device Variable Resistor

**Flash**

**Emerging NVM**
Memory & Storage Hierarchy

- **Storage**: HDD, NAND
- **Storage-Class Memory**: ReRAM, PCM
- **Non-Volatile**: DRAM, STT-MRAM, SRAM
- **Volatile**: DRAM, SRAM

<table>
<thead>
<tr>
<th>Die Cost ($/GB)</th>
<th>Access Time (sec)</th>
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</thead>
<tbody>
<tr>
<td>0.01</td>
<td>1.E-09</td>
</tr>
<tr>
<td>0.1</td>
<td>1.E-08</td>
</tr>
<tr>
<td>1</td>
<td>1.E-07</td>
</tr>
<tr>
<td>10</td>
<td>1.E-06</td>
</tr>
</tbody>
</table>

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WDC Cross Point Memory Implementations

8-layer 3D cross-point array memory ca. 2002

32Gb, 24nm, 2-layer 3D cross-point array ReRAM 2013
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   • Different workloads leading to higher memory complexity
   • Is there a better way?

3 Limitations of Current Programming Models

4 Memory Centric Computing
   • A change of perspectives
   • Near and far memory

5 Conclusions | Your challenge
Persistent Memory Programming Challenges

Memory management not equipped to handle persistent state

- **Data Corruption**
  - Regular in-memory data structures have update routines to keep the data in a consistent state
  - They have no safeguards in the face of a system failure half-way through the routine
  - These routines can generate corrupted data structures if used in persistent memory

- **Persistent Memory pointer management**
  e.g., PM-pointers pointing to non-persistent memory

- **Media management**
  - Coping with errors in persistent area
  - Data durability managed at the memory level

- **Firmware and Operating System**
  - Persistence introduces Data-at-Rest security issues
  - Persistent process load / run-time linking / execute mechanism needs to address seamless process stop / re-start
The Latency Gap: Case Study

Source: Western Digital estimates
Case Study: The Data Bottleneck

Conventional Applications
- <1% misses
- Cache Access

BIG DATA Applications
- >90% misses
- Cache Access

System Energy / Time Consumption
- 10% data transfer
- Compute
- Memory Access

96% data transfer

Source: S. Wong, CCD 2015 presentation
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In Comes NVM | SCM

Conventional Wisdom
Add another layer to the hierarchy

The Opportunity
Collapse the hierarchy

SCM layer added to the stack

HDD

MS-class Mass Storage

SCM layer added to the stack

L1

L2

L3

L4

DRAM

SCM

SSD / Flash

Storage Cache Layers

Memory

x86

Power

ARM

Others

nVIDIA

Custom ASIC

FPGA
Memory Centric Computing

*Shipping computation to the data*

**Power**
Reduction in data movement count and distance

**Performance**
Parallelism, Bandwidth, and Latency

**Cost**
Low gate count embedded cores with future open ISA and tools

Works best when simple expressions computed against large number of data records
Data Centric Compute Architectures

Data Center

Rack Scale Architecture

Cheap CPUs Around PB of SCM

Client Compute

SCM complements DRAM for compute intensive clients

Mobile

Large memory requirements for Virtual Reality

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System Challenges for eNVM Technologies

Every layer in the system must change to take advantage of low-latency eNVM

**Interface**
- Standards-based interface: e.g., NVDIMM-P
- Synchronous R/W
- R/W asymmetry

**Controller**
- Low-latency controller
- ECC, wear leveling
- Encryption

**Software Stack**
- Persistent memory programming models
- User vs. kernel space implementation

**Network**
- Low-latency fabrics
- Distributed cache coherency

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Call to Action | Your Challenge

Writing system and application software that re-thinks the hierarchy

Reverse the trend to deepening memory hierarchy
.....And A Few Words about the Commercial, Real World:
When the Chips are Down, the Wafers are Up!

How Tall Would it Be?

Number of wafers produced in 2016
In Yokkaichi
When the Chips are Down, the Wafers are Up!

Mount Kilimanjaro
19,340ft

Number of wafers produced in 2016 In Yokkaichi

Burj Khalifa
2717ft

Eiffel Tower
984ft

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15nm 1Z: Highest Yields and Fastest Yield Learning

Source: WDC estimates
Elements of WDC Technology Leadership

Power, Performance

Latency, Endurance

Cost

Vertical Integration and Ecosystem

Scalability

Scale

On time, on target, all the time
The FAB 4 of Semiconductor Nirvana

Cost  Scalability  Scale  Ecosystem

Case Study
2D NAND ➔ 3D NAND Transition
Bringing the possibilities of data to life.